AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor device comprising a first semiconductor region and a second semiconductor region,

(a) wherein ~~a field effect transistor is~~ a plurality of field effect transistors are comprised of the first semiconductor region comprising ~~at least one semiconductor layer(s)~~ a plurality of semiconductor layers protruding upward from a substrate and aligned such that the channel current direction is mutually parallel, a gate electrode(s) formed via ~~an insulating film~~ insulating films such that the gate electrode(s) strides over the semiconductor ~~layer(s)~~ layers and source/drain regions provided in the semiconductor ~~layer(s)~~ layers on both sides of the gate electrode(s),whereby a channel region is formed in at least both side surfaces of the semiconductor ~~layer(s)~~ layers,

(b) wherein the second semiconductor region comprises semiconductor layers protruding upward from the substrate and placed, ~~at least~~ opposing the first semiconductor region at both ends in the direction perpendicular to a channel current direction and between the semiconductor layers in the first semiconductor region, and

the side surfaces of the semiconductor layers facing the

first semiconductor region are parallel to the channel current direction.

2. (canceled)

3. (currently amended) The semiconductor device as claimed in Claim [[2]] 1, wherein separate source/drain regions and separate gate electrodes are formed to each of the plurality of the semiconductor layers in the first semiconductor region.

4. (currently amended) The semiconductor device as claimed in Claim [[2]] 1, wherein the gate electrode(s) is formed such that the gate electrode(s) strides over at least two of the plurality of the semiconductor layers.

5. (currently amended) The semiconductor device as claimed in Claim [[2]] 1, wherein individual source/drain regions in the plurality of the semiconductor layers are electrically commonly connected and the gate electrode(s) is formed such that the gate electrode(s) strides over the commonly connected semiconductor layers.

6. (currently amended) The semiconductor device as claimed in Claim [[2]] 1, wherein the first semiconductor region further comprises a connecting semiconductor layer which protrudes upward

from the substrate and electrically commonly connects source/drain regions of at least two of the plurality of the semiconductor layers by extending in the direction perpendicular to the channel current direction; and

the gate electrode(s) is formed such that the gate electrode(s) strides over the semiconductor layers connected by the connecting semiconductor layer.

7. (canceled)

8. (currently amended) The semiconductor device as claimed in claim [[2]] 1, wherein the plurality of the semiconductor layers are aligned at even intervals in the direction perpendicular to the channel current direction.

9. (previously presented) The semiconductor device as claimed in claim 1, wherein the semiconductor layers in the second semiconductor region formed in both sides of the first semiconductor region are disposed at even intervals from the first semiconductor region.

10. (currently amended) The semiconductor device as claimed in claim 1, wherein the semiconductor ~~layer(s)~~ layers in the first semiconductor region and the semiconductor layers in the

second semiconductor region are aligned at even intervals in the direction perpendicular to the channel current direction.

11. (currently amended) The semiconductor device as claimed in claim 1, wherein the gate electrode(s) is formed, extending from over the semiconductor ~~layer(s)~~ layers in the first semiconductor region to over the semiconductor layers in the second semiconductor region.

12. (original) The semiconductor device as claimed in Claim 11, wherein a contact with the gate electrode(s) is formed over the semiconductor layers in the second semiconductor region.

13. (currently amended) The semiconductor device as claimed in claim 1, wherein at least a part covered by the gate electrode(s) in the semiconductor ~~layer(s)~~ layers in the first semiconductor region has a substantially cuboid shape.

14. (currently amended) The semiconductor device as claimed in claim 1, wherein the semiconductor ~~layer(s)~~ layers in the first semiconductor region ~~has~~ have a substantially cuboid shape.

15. (previously presented) The semiconductor device as claimed in claim 1, wherein in the channel current direction, a length of the semiconductor layers in the second semiconductor

region in both sides of the first semiconductor region is longer than a length of the gate electrode(s).

16. (currently amended) The semiconductor device as claimed in claim 1, wherein in the channel current direction, a length of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is equal to or larger than a length of the semiconductor ~~layer(s)~~ layers in the first semiconductor region.

17. (currently amended) The semiconductor device as claimed in claim 1, wherein in the direction perpendicular to the channel current direction, a width of the semiconductor layers in the second semiconductor region in both sides of the first semiconductor region is equal to or larger than a width of the semiconductor ~~layer(s)~~ layers in the first semiconductor region.

18. (previously presented) The semiconductor device as claimed in claim 1, wherein the second semiconductor region further comprises a pair of semiconductor layers which connects from one semiconductor layer to the other semiconductor layer of the semiconductor layers in both sides of the first semiconductor region such that the second semiconductor region surrounds the first semiconductor region.

19. (currently amended) A process for manufacturing a semiconductor device, comprising ~~the steps of~~:

forming fin-type semiconductor layers for forming a first semiconductor region comprising ~~at least one semiconductor layer(s)~~ a plurality of semiconductor layers protruding upward from a substrate such that direction of channel current flowing in the individual semiconductor layers is mutually parallel, and a second semiconductor region comprising semiconductor layers protruding upward from the substrate ~~at least~~ in both sides sandwiching the first semiconductor region and between the semiconductor layers in the first semiconductor region; and

forming a transistor by forming a gate electrode(s) striding over the semiconductor ~~layer(s)~~ layers in the first semiconductor region, ~~an insulating film~~ insulating films between the gate electrode(s) and at least both side surfaces of the semiconductor ~~layer(s)~~ layers and source/drain regions in both sides sandwiching the gate electrode(s) in the semiconductor ~~layer(s)~~ layers.

20. (original) The process for manufacturing a semiconductor device as claimed in Claim 19, wherein in the step of forming the fin-type semiconductor layers, the first semiconductor region and the second semiconductor region are formed such that the side surface of the second semiconductor

region in the side of the first semiconductor region is parallel to a channel current direction.

21. (previously presented) The process for manufacturing a semiconductor device as claimed in Claim 19, wherein in the step of forming the fin-type semiconductor layers, the first semiconductor region and the second semiconductor region are simultaneously formed by processing a semiconductor substrate on the substrate into a predetermined shape.

22. (original) The process for manufacturing a semiconductor device as claimed in Claim 21, wherein in the step of forming the fin-type semiconductor layers, the processing into the predetermined shape is conducted by etching the semiconductor substrate using a mask having a shape corresponding to the first semiconductor region and the second semiconductor region.

23. (currently amended) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) extends from over the semiconductor ~~layer(s)~~ layers in the first semiconductor region to over the semiconductor layers in the second semiconductor region.

24. (original) The process for manufacturing a semiconductor device as claimed in Claim 23, wherein in the step of forming the transistor, a contact with the gate electrode(s) is further formed over the semiconductor layers in the second semiconductor region to which the gate electrode(s) extends.

25. (canceled)

26. (currently amended) The process for manufacturing a semiconductor device as claimed in Claim [[25]] 19, wherein in the step of forming the transistor, a plurality of the gate electrodes are formed such that each gate electrode strides over one semiconductor layer in the first semiconductor region.

27. (currently amended) The process for manufacturing a semiconductor device as claimed in Claim [[25]] 19, wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) strides over at least two or more of the plurality of the semiconductor layers in the first semiconductor region.

28. (currently amended) The process for manufacturing a semiconductor device as claimed in Claim [[25]] 19, wherein in the step of forming the fin-type semiconductor layers, a connecting semiconductor layer is further formed as the first

semiconductor region, which protrudes upward from the substrate, extends in a direction perpendicular to the channel current direction and electrically commonly connects at least two of the plurality of the semiconductor layers; and

wherein in the step of forming the transistor, the gate electrode(s) is formed such that the gate electrode(s) strides over the semiconductor layers connected by the connecting semiconductor layer.

29. (canceled)

30. (currently amended) The process for manufacturing a semiconductor device as claimed in claim [[25]] 19, wherein in the step of forming the fin-type semiconductor layers, the plurality of the semiconductor layers in the first semiconductor region are formed at even intervals in the direction perpendicular to the channel current direction.

31. (currently amended) The process for manufacturing a semiconductor device as claimed in claim [[25]] 19, wherein in the step of forming the fin-type semiconductor layers, the semiconductor layers in the second semiconductor region are disposed in both sides of the first semiconductor region at even intervals from the first semiconductor region.

32. (currently amended) The process for manufacturing a semiconductor device as claimed in claim [[25]] 19, wherein in the step of forming the fin-type semiconductor layers, the plurality of the semiconductor layers in the first semiconductor region and the semiconductor layers in the second semiconductor region are formed at even intervals in the direction perpendicular to the channel current direction.

33. (currently amended) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step of forming the fin-type semiconductor layers, at least a part covered by the ~~electrode gate(s)~~ gate electrode(s) in the semiconductor ~~layer(s)~~ layers in the first semiconductor region [[are]] is formed such that the part has a substantially cuboid shape.

34. (currently amended) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step of forming the fin-type semiconductor layers, the semiconductor ~~layer(s)~~ layers in the first semiconductor region are formed such that the semiconductor ~~layer(s) has~~ layers have a substantially cuboid shape.

35. (previously presented) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step

of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a length of the semiconductor layers in the channel current direction is longer than a length of the gate electrode(s).

36. (currently amended) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a length of the semiconductor layers in the channel current direction is longer than a length of the semiconductor ~~layer(s)~~ layers in the first semiconductor region.

37. (currently amended) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step of forming the transistor, the semiconductor layers in the second semiconductor region are formed in both sides of the first semiconductor region such that a width of the semiconductor layers in the direction perpendicular to the channel current direction is equal to or larger than a width of the semiconductor ~~layer(s)~~ layers in the first semiconductor region.

38. (previously presented) The process for manufacturing a semiconductor device as claimed in claim 19, wherein in the step of forming the fin-type semiconductor layers, a pair of semiconductor layers are further formed as the second semiconductor region, which connects from one semiconductor layer to the other semiconductor layer of the semiconductor layers in both sides of the first semiconductor region such that the second semiconductor region surrounds the first semiconductor region.